

MARKED-UP COPY OF AMENDED CLAIMS:

9. (AMENDED) A method of enhancing the reliability of electrical connections in a semiconductor package during operation of the chip, comprising the steps of:

(a) providing a semiconductor chip having a front ~~contact-bearing~~ surface and a rear surface, said front surface having contacts;

(b) providing flexible leads extending from said contacts on said front surface of said chip by wire bonding, said flexible leads being connected to said contacts at joints on said front surface;

(c) ~~juxtaposing~~ placing a spreader above said front surface, said spreader having a coefficient of thermal expansion substantially equal to the coefficient of thermal expansion of said chip; and

(d) disposing a liquid encapsulant between said front surface and said spreader and around said leads and curing said encapsulant, whereby the motion of the leads during thermal cycling ~~leads~~ is constrained.

10. (AMENDED) The method as claimed in claim 9, further comprising the step of providing a predetermined geometry for the cured encapsulant so as to affect the ~~constraint~~ constraint of the leads.

REMARKS

The present communication is responsive to the Official Action mailed August 30, 2001. A petition for a three-month extension of the term for response to said Official Action, to and including February 28, 2002, is transmitted herewith.

Claims 9 and 10 were rejected under 35 U.S.C. § 112, ¶ 2. The Examiner's points in this rejection are well taken, and these claims have been amended in response thereto. Also, to further clarify step (c) of claim 9, the phrase "juxtaposing a spreader above said front surface" has been modified to read "placing a spreader above said front surface."

Claims 1-3 were rejected under 35 U.S.C. § 103(a) as unpatentable over *Degani et al.*, U.S. Patent 5,473,512 ("*Degani* '512") and *DiStefano*, U.S. Patent 5,834,339 ("*DiStefano* '339") in combination with one another. Reconsideration and withdrawal of this rejection are respectfully requested. *DiStefano* '339 is not legally available as prior art against the claims of the present application. *DiStefano* '339 issued on November 10, 1998, after the filing date of U.S. Patent Application 08/962,988, the direct parent of the present application. Manifestly, *DiStefano* '339 is not available as prior art under 35 U.S.C. § 102(a) or § 102 (b). At the time the inventions presently claimed were made, both the presently-claimed inventions and U.S. Patent Application 610,610, which resulted in the *DiStefano* '339 patent, were owned by, or subject to an obligation of assignment to, Tessera, Inc. ("Tessera"). Tessera is the assignee of the present application and is also the assignee of the *DiStefano* '339 patent. It is noted that the present application was filed after November 29, 1999. Accordingly, 35 U.S.C. § 103(c) precludes a 35 U.S.C. § 103/102(e) rejection. M.P.E.P. § 706.02(1)(1) and (2).

Claims 4-8 were rejected under 35 U.S.C. § 103(a) as unpatentable over *DiStefano* '339 in view of *Degani* '512. For exactly the same reasons as discussed above, this rejection is also believed to be precluded by 35 U.S.C. § 103(c) and its withdrawal is respectfully requested.

Claims 9 and 10 were rejected under 35 U.S.C. § 102(b) on *Ueda*, U.S. Patent No. 5,157,478 ("*Ueda* '478"). By the present amendment, claim 9 has been amended to state that the step of providing flexible leads extending from the contacts on the front surface of the chip is performed "by wire bonding." *Ueda* '478 is specifically directed to particular problems encountered in a TAB assembly. See col. 1, lns. 10-16. Accordingly, a § 102 rejection is inapplicable to claim 9 as amended or to claim 10.

New claims 11 and 12 further specify the geometry of the cured encapsulant. See Fig. 7 of the present drawings. New claims 13 and 14 further specify the step of providing the flexible leads by wire bonding as forming the bonding wire into loops projecting upwardly away from the front surface (claim 13) and further including downwardly projecting portions extending from the loops and extending downwardly beyond the front surface of the chip (claim 14). This arrangement is seen, for example, in Figs. 1-4 and 6-8 of the present drawings. These claims are believed to distinguish over *Ueda* '478 for the same reasons as advanced above in connection with claim 9, and further to distinguish over *Ueda* '478 by virtue of the specific features recited therein.

New independent claim 15 is similar to claim 9 but does not specifically recite the use of wire bonding. New claim 15, however, recites positioning the semiconductor chip relative to an "element having conductive features thereon" so that the element extends "beneath said rear surface of said chip" and so that the front or contact-bearing surface of the chip faces

"upwardly away from said element." Further, claim 15 recites providing the flexible leads extending "downwardly to said element." These features are exemplified in all of the present drawings. For example, leads 54 (Fig. 1) extend downwardly to element 20, whereas leads 254 (Fig. 5) extend downwardly to element 220. Ueda '478 is not seen as teaching any such arrangement or as suggesting anything appropriate to construction of such an arrangement. New dependent claims 16 and 17 specifically recite wire bonding as discussed above.

As it is believed that all of the objections, rejections and requirements set forth in the Official Action have been fully met by the foregoing amendments and remarks, favorable reconsideration and allowance of all claims in the application are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: February 26, 2002

Respectfully submitted,

By 

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